IN THE CLAIMS:

Please amend the claims as follows:

1. (Previously Presented) Slave circuit which can be connected in series with further slave circuits and a master circuit to form a ring structure, having:

(a) a data transmission interface for processing data frames which are received from the master circuit, where the data transmission interface has an external data input for receiving the data frames from the master circuit and a data output for sending data frames to the next series connected slave circuit, where each data frame contains at least a first data field for an address and a second data field for transmitting user data;

(b) an address register for storing an address, where the address register has stored, prior to the initialization of the slave circuit by the master circuit, a predetermined initialization address which is provided for all the slave circuits jointly;

(c) a comparator for comparing the address stored in the address register with an address received from the data transmission interface in a data frame, where the address register stores the data transmitted in the second data field of the data frame as a future address for the slave circuit if the address transmitted in the first data field of the data frame is identical to the predetermined initialization address;

(d) an indicator register which indicates the initialization of the slave circuit if the address received by the data transmission interface in the slave circuit is identical to the predetermined initialization address; and having

(e) an inhibit logic unit which inhibits the data output of the data transmission interface until the indicator register indicates initialization of the slave circuit.

2. (Previously Presented) Slave circuit according to claim 1, wherein the data transmission interface has a data output for sending data, an internal data output for sending the data extracted from the received data frame in line with a data transmission protocol to a data processing unit, an internal address output for sending the address extracted from the received data frame in line with the data transmission protocol to the data processing unit, and a clock signal input for receiving a clock signal.

3. (Currently Amended) Slave circuit according to claim [[5]]1, wherein the indicator register is a flipflop which is actuated by the comparator.

4. (Previously Presented) Slave circuit according to claim 1, wherein the data output is at logic high in the inactive state of the data transmission interface, and in that the indicator flipflop is at logic high if the slave circuit has not been initialized.

5. (Previously Presented) Slave circuit according to claim 4, wherein the inhibit logic unit has:

(a) an OR gate, whose first input is connected to the external data input of the data transmission interface and whose second input is connected to the indicator flipflop, and

(b) an AND gate, whose first input is connected to the output of the OR gate and whose second input is connected to the data output of the data transmission interface.

6. (Previously Presented) Slave circuit according to claim 1, wherein the inhibit logic unit has a synchronization flipflop connected downstream of it.

7. (Previously Presented) Slave circuit according to claim 6, wherein when the slave circuit is connected in series with a further slave circuit the respective output of the synchronization flipflop in a slave circuit is connected to the external data input of the further downstream slave circuit.

8. (Previously Presented) Slave circuit according to claim 7, wherein when the slave circuits are connected in series with the master circuit to form a ring structure the external data input in the first slave circuit is connected to a data output on the master circuit, and the output of the synchronization flipflop in the last slave circuit is connected to a data input on the master circuit.

9. (Previously Presented) Slave circuit according to claim 1, wherein the slave circuit is an integrated circuit having three connections, namely a first connection, which is connected to the data input of the data transmission interface, a second connection, which is connected to the output of the synchronization flipflop, and a third connection, which is connected to the clock input of the data transmission interface and to the clock input of the synchronization flipflop.

10. (Previously Presented) Slave circuit according to claim 1, wherein the data transmission protocol for processing the transmitted data frames is an HDLC protocol.

11. (Canceled)